CLAIMS

CLAIM 1

In a method for addressing and sustaining a PDP wherein an addressing voltage is applied to at least one section S1 of the PDP while at least one other section S2 of the PDP is being simultaneously sustained, the improvement wherein visual artifacts between the sections are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

CLAIM 2

In a method for operating a surface discharge AC plasma display having row scan, bulk sustain, and column data electrodes, the improvement which comprises addressing at least one section S_1 of the AC plasma display while another section S_2 is being simultaneously sustained, each section having a predetermined number of bulk sustain electrodes and row scan electrodes, and wherein visual artifacts between the sections are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

CLAIM 3

The invention of Claim 2 wherein section S_2 is subsequently addressed while section S_1 is being sustained.

CLAIM 4

The invention of Claim 3 wherein there are 6 to 17 subfields

CLAIM 5

The invention of Claim 4 wherein each of the sections S_1 and S_2 is sustained with a different number of sustains per subfield.

CLAIM 6

The invention of Claim 4 wherein at least one subfield of each section S1 and S2 is sustained with the same number of sustains per subfield.

CLAIM 7

The invention of Claim 2 wherein the resolution of the plasma display is about 480 to about 1200 row scan electrodes.

CLAIM 8

The invention of Claim 2 wherein there are 6 to 17 subfields for a resolution up to 768 row scan electrodes.

CLAIM 9

The invention of Claim 2 wherein the method for the reduction of motion and visual artifacts includes the writing of pixels followed by selective erase.

CLAIM 10

The invention of Claim 1 wherein there is provided a reset voltage before addressing.

CLAIM 11

The invention of Claim 10 wherein the reset before addressing is a slow ramp reset voltage.

CLAIM 12

An AC plasma display having row scan, bulk sustain, and column data electrodes, said display being divided into a plurality of sections S_1, S_2, S_n, each section having a predetermined number of bulk sustain electrodes and row scan electrodes, and electronic circuitry for simultaneously addressing and sustaining at least two different sections of the AC plasma display, the improvement wherein visual artifacts between a section being addressed and a section being simultaneously sustained are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between the sections.

CLAIM 13

The invention of Claim 12 wherein there is provided a reset voltage before addressing.

CLAIM 14

The invention of Claim 13 wherein the reset before addressing is a slow ramp reset voltage.

CLAIM 15

In a system for addressing and sustaining PDP, wherein an addressing voltage is applied to at least one section S1 of the display panel while at least one other section S2 of the panel is being simultaneously sustained, the improvement wherein visual artifacts are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between S1 and S2.

CLAIM 16

In a system having electronic circuitry for operation of an AC plasma display having row scan, bulk sustain, and column data electrodes, said display being divided into a plurality of sections S_1, S_2, S_n, each section having a predetermined number of bulk sustain electrodes and row scan electrodes the improvement which comprises electronic circuitry for simultaneously addressing

and sustaining at least two different sections of the AC plasma display and wherein visual artifacts between a section being addressed and a section being simultaneously sustained are reduced by means of gamma corrected subfields with sustains timed to balance the center of light between the sections.

Claim 17

The invention of Claim 16 wherein there is provided a reset voltage before addressing.

Claim 18

The invention of Claim 17 wherein the reset before addressing is a slow ramp reset voltage.

Claim 19

In a method for reducing visual artifacts in a display, the improvement wherein gamma curves are applied based on frame and spatial position.

Claim 20

The invention of Claim 19 wherein the display contains a plurality of pixels and wherein gamma correction is applied to one or more pixels of the display, said gamma correction being applied to each pixel based on time and spatial position.

Claim 21

The invention of Claim 20 wherein pixels are selectively grouped for gamma correction and a unique gamma curve is separately applied to the input luminance of each pixel in the group, each gamma curve being shaped such that only a limited number of pixels are allowed to change in response to incremental changes in the input luminance while the other pixels in the group remain constant.

Claim 22

The invention of Claim 20 wherein pixels are selectively grouped for gamma curve correction, a separate gamma curve being applied to the input luminance of each pixel, each gamma curve being shaped so as to prevent simultaneous changes in all of the pixels when the input luminance of the pixels increases from n to n+1 or decreases from n to n-1, where n is the input luminance value.

Claim 23

The invention of Claim 21 wherein four pixels are selectively grouped in a two pixel by two pixel quadrant so as to act in concert, a different gamma curve being applied to the input luminance of each pixel, the slope and characteristics of each gamma curve being such that only one pixel changes while the other pixels in the group remain unchanged.

Claim 24

In a method for addressing a matrix of pixels or subpixels in a display, wherein pixels are selectively grouped for gamma correction, the improvement wherein only a limited number of pixels are changed while the other pixels are simultaneously unchanged such that motion artifacts including false contour are reduced.

Claim 25

In a method for reducing artifacts in a display in which the Floyd Steinberg method is used to produce error diffusion, the improvement which comprises including a random term to improve contrast at low luminance.

Claim 26

The method of Claim 25 in which the weighting value of each product term varies in accordance with time and position.

Claim 27

The method of Claim 26 in which the error diffusion is applied simultaneously and independently to two pixels adjacent on a row such that neither of the resultant error terms is included in the calculation of the error term of the other pixel.

CLAIM 28

In a method for reducing artifacts wherein dithering is used, the improvement wherein a dither matrix of at least 4 x 4 pixels is used and the dither coefficients are optimized based on input luminance, the coefficient being selected to evenly distribute the gray scale dither pattern over the matrix.

CLAIM 29

The invention of Claim 28 wherein the dither coefficients are selected in such a way as to limit the carry value added to the upper bits when summed with the dither bits of the input luminance and the carry bit from the error diffusion.

CLAIM 30

The invention of Claim 29 wherein the dither coefficients are selected such that any single pixel is toggling between n and n+1 when the same input luminance is applied to the matrix.

Claim 31

In a method for reducing artifacts in a display, the improvement wherein the timing of light pulses emitted by the display is controlled such that the center of light gravity or mass increases monotonously with increasing input luminance.

Claim 32

The invention of Claim 31 wherein the timing of subfields is adjusted.

Claim 33

The invention of Claim 31 wherein the weighting of subfields is adjusted

Claim 34

The invention of Claim 31 wherein the display is a digital micromirror device.

Claim 35

The invention of Claim 31 wherein the display is an inorganic or organic electroluminescent device.

Claim 36

The invention of Claim 31 wherein the display is a passive LCD, a passive matrix LCD, or an active matrix LCD.

Claim 37

The invention of Claim 31 wherein the display is a ferroelectric liquid crystal device.

Claim 38

The invention of Claim 31 wherein the display is an organic electroluminescent or organic light emitting diode device.

Claim 39

The invention of Claim 31 wherein the display is a liquid crystal on silicon device.

Claim 40

The invention of Claim 31 wherein the display is a DC plasma device.

Claim 41

The invention of Claim 31 wherein the display is an AC plasma display device.

Claim 42

In an integrated circuit (IC) for receiving and processing digital signals to a display, the improvement wherein the processing comprises one or more artifact reduction methods including gamma correction, error diffusion, and/or dithering.

Claim 43

The invention of Claims 42 wherein the IC processing includes timing functions.

Claim 44

The invention of Claim 43 wherein SAS architecture is processed within the same or a different IC.

Claim 45

In an integrated circuit for receiving and processing digital signals to a display, the improvement wherein the processing includes SAS.

Claim 46

The invention of Claim 45 wherein the processing includes the center of light method.

Claim 47

In a display employing gamma correction, error diffusion and/or dithering functions, the improvements wherein the functions are processed in a single integrated circuit.

Claim 48

The invention of Claim 47 in which the integrated circuit receives input data from a video source, synchronizing signals from the timing and control electronics, and sends the output data to a frame buffer.

Claim 49

The invention of Claim 48 in which the frame buffer is included in the integrated circuit, and the integrated circuit communicates directly with the data drive circuitry.

Claim 50

The invention of Claim 48 in which the synchronizing signals for the timing and control electronics are included in the integrated circuit and the integrated circuit communicates directly with the data drive circuitry and the sustain and waveform timing.